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Analysis of charge sharing in MOSFET's in view of available scaling trends

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Abstract : *The error voltage induced by the turning off of an MOS switch is one of the fundamental factors that limit the accuracy of switched-capacitor circuit. The induced error voltage is a phenomenon arising due to the presence of static charges in the MOSFET channel which further gives rise to Charge Sharing/Charge Injection at the time of switching off of the MOSFET. Charge injection thus has a dependence on the amount of charge present in the MOSFET channel which further is a function of different parameters.*
The aim of this paper is to study the variation of linear charge density (charge per unit length) with the channel length for all the available scaling trends. As the linear charge density is a function of parameters such as channel length, substrate doping and the oxide thickness, which are the primary subjects of change in different scaling techniques. Therefore, the behaviour of the linear charge density with different scaling techniques has been studied and compared. Further analytical modelling has been carried out and the magnitudes of linear charge densities for the three cases with the application of respective scaling trends have been plotted and compared.

Keywords – *Charge Sharing, Error Voltage, Linear Charge Density, MOSFET, Scaling*

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I. Introduction

The technology involved in various fields of devices has undergone a tremendous change in past few decades. Older concepts and design techniques are paving way for new and better design procedures. VLSI and related field are no exception to this revolution in technology. Various factors that have been kept in mind while floating new ideas of design and implementation are the cost, performance, power dissipation and speed etc. Due to advances in the manufacturing technology chips carrying a lot of components and performing a lot of vital functional have been realizable. All these factors (speed, performance etc) do affect various other characteristics of device i.e., the device performance in some way or the other does get affected by the manipulations and innovations that are resorted to achieve better results for the devices. A lot of techniques have been put to use in order to achieve the best results, scaling being one of them. It has aided a lot in achieving a better performance at minimal costs with an optimum speed of operation. But better performance of the devices is achieved at the cost of other factors as well. Similar is the case with the device of interest i.e. MOSFET. As MOST's are having very high input impedance which performs excellent holding functions and hence find application in sample and hold circuits. But when MOSFET is used as a switch in sample and hold circuits, the main problem that arises is that of Charge Sharing. Charge sharing gets its name from the fact that the charge present in a MOSFET channel is shared by the input node and the output node or a hold capacitor whatever the case may be during switching action of the MOSFET. This sharing of charge gives rise to an additional voltage "error voltage, ΔV" on the capacitor side. This error voltage limits the accuracy of the high performance analog CMOS circuits as they need large transistors (which invoke high channel charge) and small capacitors to reduce the transfer time constant. The prediction of the error voltage ΔV will be based on the following qualitative physical description of the charge injection phenomenon in MOS transistor. A rapid variation of the gate voltage causes a variation of the surface potential as the amount of mobile charges cannot change instantaneously. The surface potential induces an immediate variation of the depletion width, which compensates the excessive charge. Equilibrium corresponding to the new gate voltage is reached by the subsequent charge flow to drain and source. A fraction of charge in the channel escapes to the substrate leading to the charge pumping which is due to the recombination in the channel and into the substrate.

The concept of charge sharing was first presented by Bing and Chenming [1] and had derived a concise analytical expression for switch-induced error voltage on a switched capacitor from the distributed MOSFET

model. Even before that David Macquigg had presented a semi-empirical model for the estimation of residual charge on a Switched Capacitor [2]. Universal charge injection model was developed by Yongwang Ding and Ramesh Hirjani [3]. A new approach was presented for minimization of the charge injection in switched-current circuits by removing the charge before the charge injection could actually occur. [4]. Wenwei Yang, Yuehui Yu, Zhiping Yu, Lilin Tian presented an analysis of SOI RESURF structure with charge sharing concept [5]. Kewei Yang and Andreas G.Andreou presented the concept of a multiple input differential amplifier based on the charge sharing on a floating-gate MOSFET [6]. Further, a new quantitative model for weak inversion charge injection in MOSFET analog switches was presented [7]. The model was derived at the critical point where the device is operated in the transition region between strong inversion and weak inversion. The concept of floating-gate charge sharing which was put forward was a novel circuit for Analog Trimming [8]. A floating gate charge-sharing circuit that can be electrically programmed for precise positive and negative voltage changes, and can be implemented in a standard CMOS VLSI process was also presented. This novel and attractive idea of developing a low power SRAM design was floated using charge sharing technique [9]. By reducing the bitlines voltage swing, the bitlines dynamic power has been reduced. Low-Power design of high-capacitive CMOS circuits using a new charge sharing scheme has been presented [10]. In CMOS ICs, reducing VDD reduces dynamic power quadratically. A non-quasi static transient model of Fully-Depleted SOI MOSFET and its application to the analysis of charge sharing in analog switches has been developed [11]. In this paper fast one-dimensional numerical model suitable for circuit analysis has been developed for fully-depleted SOI MOSFETs. C. H. Cheng, S. C. Chang, J. S. Wang, and W. B. Jone presented a method of Charge Sharing Fault Detection for CMOS Domino Logic Circuits [12]. Because domino logic design offers smaller area and higher speed than conventional CMOS design. It is very popular in high performance processor design. The decreasing feature size has enabled single event charge sharing [13], i.e. multiple devices collecting charge from the charge cloud created by an incident ion. While charge sharing can be detrimental to storage cells, it can be beneficial in combinatorial circuits in which pulse quenching occurs. Duan Xueyan, Wang Liyun, and Lai Jinmei presented four types of pulse quenching mechanism for the first time, in commonly used logic gates and verified them using 3-D TCAD mixed mode simulations in a commercial 90 nm CMOS process. Pengcheng Huang, Shuming Chen, Jianjun Chen, Liang Bin, Zhenyu Wu presented a novel seamless guard band (SGB) technique for charge sharing mitigation using 3-D TCAD numerical simulations [14]. The simulations results indicate that the SGB technique can not only mitigate the single-event transient pulsewidth greatly but also mitigate the charge sharing between logical nodes or logical cells significantly. An analytical model has been designed for the subthreshold slope degradation of localized-charge-trapping based non-volatile memory devices [15]. The model incorporates fringing field effects and asserts that the subthreshold slope degradation is a distinct characteristic of localized-charge-trapping.

The aim of this paper is to study the effects on linear charge density in case of sub micron MOSFETS, because the charge that comes on the hold capacitor due to charge sharing comes from the channel itself.

II. The Problem Description

The error voltage induced by the turning off of an MOS switch is one of the fundamental factors that limit the accuracy of switched-capacitor circuits, such as analog-to-digital converters, digital-to-analog converters and filters. There has been an extensive study of the dependence of this error phenomenon on different process parameters of the MOSFET. The induced error voltage is a phenomenon arising due to the presence of static charges in the MOSFET channel. The process parameters on which the error voltage depends include gate voltage falling rate, signal voltage level, the substrate doping, oxide thickness, source impedance and in general the device dimensions. The fundamental parameter amongst the above which would dictate much of the influence on the magnitude of the charges present in source-drain channel is the length of the channel itself. The length of the channel is a direct indication of the relative magnitude of the charge present in it. Thus the amount of charge present in the source-drain channel is directly proportional to the length of the channel. This inference is correct to the extent of evaluating the dependence of the error voltage on channel length only as was shown by Bing J. Sheu and Chenming Hu [1]. But the technology is not subjected to the change of a particular dimension independent of the other related features. In the practical world of device manufacturing and technological advancement one cannot change the MOSFET channel length without taking into account the change in the other related features affecting the MOSFET behaviour. The change in the MOSFET dimensions and other parameters go in accordance with some formal laws known as the scaling trends. These scaling trends define the change in all the MOSFET parameters feasible for attainment of a particular situation say for example with regard to the intensity of electric fields or regarding the behaviour of threshold voltage. But in all the scaling trends, with the scaling down of the source-drain channel length the substrate doping is always increased to prevent breakdown because the voltages are never scaled with the same factor. So as to mitigate the effects of channel length or oxide thickness decrease on the intensity of the electric fields present in the conducting channel the substrate doping increases which in turn mean that there would be a change in the channel charge density and more likely so towards the increasing side. This opens up a greater avenue for studying the problem

of charge injection in the MOSFETs taking into account the effect of the overall scaling phenomenon. The scaling involves, with the decrease of channel length, an increase in the substrate doping and a decrease in the gate oxide thickness. Again there is a possibility of channel charge density showing a change with the gate voltage level variation above threshold.

The theoretical insight into the problem leads one to believe that the variation characteristic of the linear channel charge density should be reflected the same way in the charge injection phenomenon. This is so because charge injection is found to have a direct dependence on gate voltage falling rate and it is found to be more for fast falling rates [1]. This property can actually be attributed to the amount of time the channel charge gets to get distributed between the source, the drain and the substrate. As the increase in the channel charge density would lead to an increase in the relative percentage of channel charge going towards the drain region because with the increased density channel charge would have a relatively lesser time even if the same gate clock is used. Thus the increase in linear channel charge density should lead to a relative increase in the effects of charge injection. This can be verified by carrying out the simulations and analyzing the dependence by some graphical methods. Also the possibility of channel charge density dependence on the source-drain voltage could be explored.

III. Results And Discussions

In this paper effort has been made to reconcile the initial comprehensions with the practical behaviour of the MOSFET by analytical modelling of the device parameters and also by carrying out simulations of its model in ORCAD.

3.1 Analytical Modelling

Here the variation of linear charge density (charge per unit length) with the channel length for all the available scaling trends has been explored. Further effort has been made to explore if there is any appreciable variation in the channel charge density with the magnitude of applied gate voltage above threshold.
From the MOSFET physics [16], at strong inversion linear charge density is given by:

$$Q_{invL} = \frac{\sqrt{2qN_A \in_{si} KT \ln \frac{N_A}{n_i}}}{L} \quad (1)$$

As the amount of charge present in the inversion layer is a direct function of the voltage applied at the gate above the threshold level, therefore to account for the effect of the magnitude of the gate voltage above the threshold level on the channel charge density, factor which in effect is the product of the gate capacitance and the gate voltage above threshold has been incorporated in equation 1. Therefore, with the effect of gate voltage linear charge density in the channel after strong inversion would be:

$$Q'_{invL} = \frac{\sqrt{2qN_A \in_{si} KT \ln \frac{N_A}{n_i}} + \in_{ox} \frac{A}{d}(V - V_{th})}{L} \quad (2)$$

where: L: MOSFET channel length, q: Electronic charge, NA: Substrate doping, $\in_{si}$: Permittivity of silicon, $\in_{ox}$: Gate oxide permittivity, d: Oxide thickness, A: Gate area, V: Applied gate voltage, Vth :Threshold voltage, T: Absolute temperature, K: Boltzman constant

The linear charge density, as seen from equations 1 and 2, is a function of parameters such as channel length, substrate doping and the oxide thickness which are the primary subjects of change in different scaling techniques. Qinv will change as according to the type of scaling technique under consideration. Therefore, the behavior of the linear charge density with different scaling techniques has been studied and further compared.

3.1.1 Behavior with fixed voltage scaling:

In this type of scaling the voltages are not scaled. The length has been scaled by a factor, say S, S>1, i.e. L` = L/S. In order to prevent breakdown, substrate doping has been enhanced. Also the gate oxide thickness gets scaled down with the same factor S. For this type of doping we have

$$N'_A = S^2 N_A$$

Therefore, for fixed voltage scaling, new linear charge density at strong inversion is given by:

$$Q_{invLFV} = \frac{\sqrt{2qS^2N_A \in_{si} KT \ln \frac{S^2N_A}{n_i}}}{\frac{L}{S}} \quad (3)$$

Indicating that in effect the equation 1 gets multiplied by a factor greater than $S^2$and hence the linear charge density increases with this type of scaling for strong inversion region.
Also, new linear charge density with the effect of gate voltage above threshold is given by:

$$Q'_{invLFV} = \frac{\sqrt{2qS^2N_A\epsilon_{si}KT\ln\frac{S^2N_A}{n_i}}+\epsilon_{ox}\frac{\frac{A}{S^2}}{\frac{d}{S}}(V-V_{th})}{\frac{L}{S}} \quad (4)$$

This shows that the first part of the sum is again multiplied by a factor greater than S^2 whereas the second part does not witness any change which in effect leads us to infer that there is a net increase in linear charge density even after considering the effect of gate voltage above the threshold level.

3.1.2 Behavior with constant field scaling:

In this type of scaling both the threshold voltage and the channel length are scaled by the same factor, say S and S>1. The gate oxide thickness also gets scaled down by the same factor. Thus we have:

$$L' = \frac{L}{S}$$
$$V'_{th} = \frac{V_{th}}{S}$$
$$N'_A = N_A \times S$$

Thus considering the above discussed scaling behaviour, linear charge density at strong inversion for constant field scaling is given by:

$$Q_{invLCF} = \frac{\sqrt{2qSN_A\epsilon_{si}KT\ln\frac{SN_A}{n_i}}}{\frac{L}{S}} \quad (5)$$

Thus equation 1 in effect gets multiplied by a factor more than $S^{1.5}$, indicating that the linear charge density increases in this type of scaling also at the strong inversion.

Also, for the same scaling behavior new linear charge density, considering the effect of the gate voltage above threshold,

$$Q'_{invLCF} = \frac{\sqrt{2qSN_A\epsilon_{si}KT\ln\frac{SN_A}{n_i}}+\epsilon_{ox}\frac{\frac{A}{S^2}}{\frac{d}{S}}\left(V-\frac{V_{th}}{s}\right)}{\frac{L}{S}} \quad (6)$$

Here also the first part of the sum in equation 2 gets multiplied by a factor more than S1.5 whereas the second part also witnesses a decrease in threshold voltage. Thus there is a net increase in linear charge density even after taking into account the effect of gate voltage above threshold level.

3.1.3 Behavior with general scaling:

In this type of scaling of scaling the voltages and the device dimensions has been scaled down by different factors. If dimensions are scaled by a factor say S then the voltages are scaled by some other factor say U where S>1, U>1. The relation between U and S is not explicit. Therefore in this case:

$$L' = \frac{L}{S}$$
$$V_{th} = \frac{V_{th}}{U}$$
$$N'_A = N_A \times \frac{S^2}{U}$$

Thus including the scaling factors discussed above, new linear charge density for general scaling at strong inversion is given by,

$$Q_{invLG} = \frac{\sqrt{2q\frac{S^2}{U}N_A\epsilon_{si}KT\ln\frac{\frac{S^2}{U}N_A}{n_i}}}{\frac{L}{S}} \quad (7)$$

Thus for this case the equation 1 is in effect multiplied by a factor greater than S2/U0.5, Indicating that the linear charge density increases in this type of scaling also at the strong inversion.

Also for the same scaling behavior new linear charge density considering the effect of gate voltage above threshold,

$$Q'_{invLG} = \frac{\sqrt{2q\frac{S^2}{U}N_A\epsilon_{si}KT\ln\frac{\frac{S^2}{U}N_A}{n_i}}+\epsilon_{ox}\frac{\frac{A}{S^2}}{\frac{d}{S}}\left(V-\frac{V_{th}}{U}\right)}{\frac{L}{S}} \quad (8)$$

In this case also the first part of the sum increases with the multiplication of a factor greater than $S^2/U^{0.5}$ and the threshold voltage also witnesses a decrease for the second part of the sum in equation 2.This indicates that there is an increase in linear charge density even after considering the effect of gate voltage above threshold.

3.1.4 Comparison of the three techniques:

In analytical modelling, for the linear channel charge density, three different equations have been obtained for both the strong inversion region and the one taking into account the value of the gate voltage above the threshold level into the saturation region for all the three different types of scaling behaviors. Further, the relative magnitudes of linear charge densities as a function of channel lengths with the application of respective scaling trends have been plotted in figure 1.

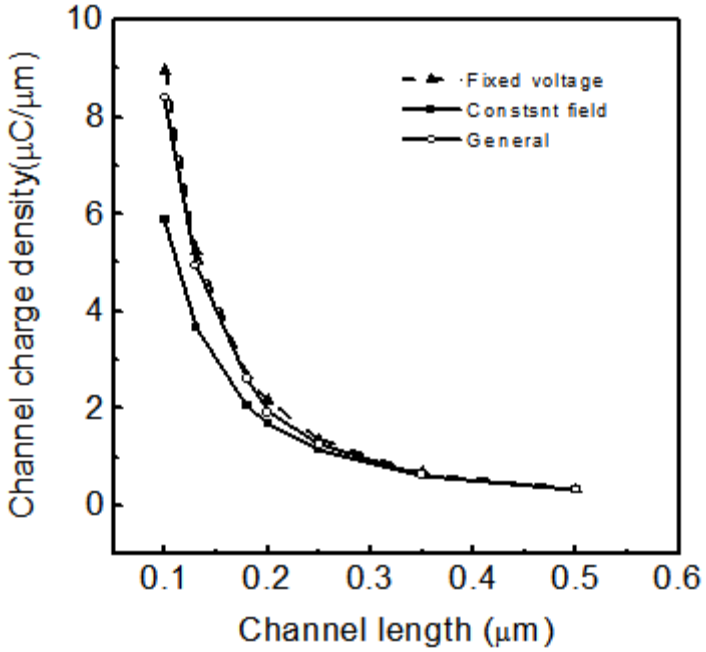


Figure 1: Linear channel charge density as a function of channel length for three types of scaling techniques

This process has been carried out in MATLAB from which different parameter values have been calculated for all the three types of scaling behaviors. Further, a graph has been plotted to obtain a relative comparison of the three techniques with respect to the different parameter values at different technology nodes in the practical world of VLSI design in the three types of scaling trends. .

It has been observed that, as was concluded from the equations 3, 5, 7, the channel charge density increases with the decrease in channel length. The increase in the density is steeper towards the nanometer regime and this behavior is observed for all the three types of scaling methods. The curve for constant field scaling lies below the other two by a relatively considerable amount which means that constant field scaling behavior guarantees the minimal amount of the error voltage for a given value of device dimensions. Further, the curves for fixed voltage and general scaling behaviors are almost coincident. Thus for the phenomenon of charge injection these two techniques yield almost similar results.

3.2 Simulation Results

The simulations have been carried out in the LEVEL 3 of PSPICE MOSFET model [17]. The following simulations attempt to study the transient behaviour of the drain current with the change in the MOSFET channel length towards the submicron dimensions. The channel width and all other parameters have been fixed for some standard value and the length of the channel has been scaled to lower values. The PSPICE schematic used is shown in the figure 2. Schematic shown in figure 2 has been simulated for the peak drain current for different values of channel lengths and the corresponding threshold voltage as dictated by the scaling trends. The MOSFET channel length is the primary subject of scaling for all the three types of scaling trends and for scaling down the parameter it is divided by a factor S, S>1. The threshold voltage is not scaled down in case of constant voltage scaling where as it gets scaled down, though not proportionally for the other two types of scaling methods.

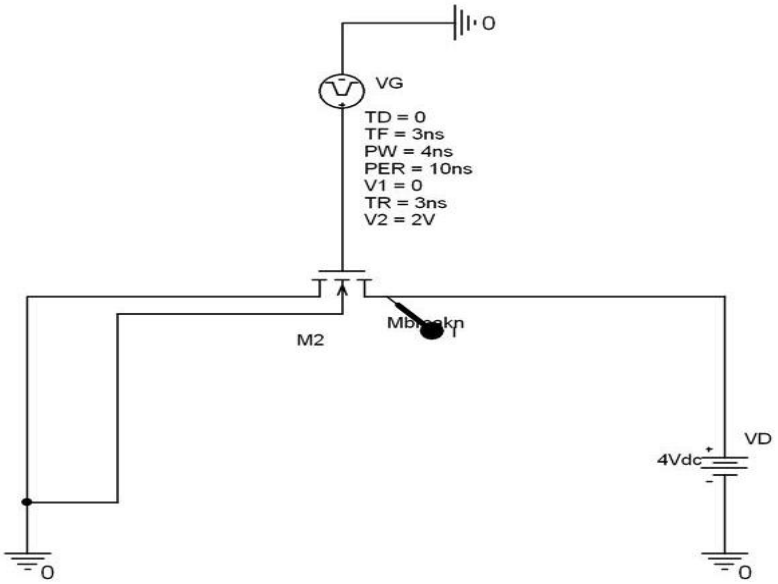


Figure :2 PSPICE schematic for transient characteristics

3.2.1 Drain current with constant voltage scaling: Figure 3 shows a typical simulation output profile for the transient characteristics of the drain current. The transient characteristics have the same shape for all different channel lengths except for the rate of fall.

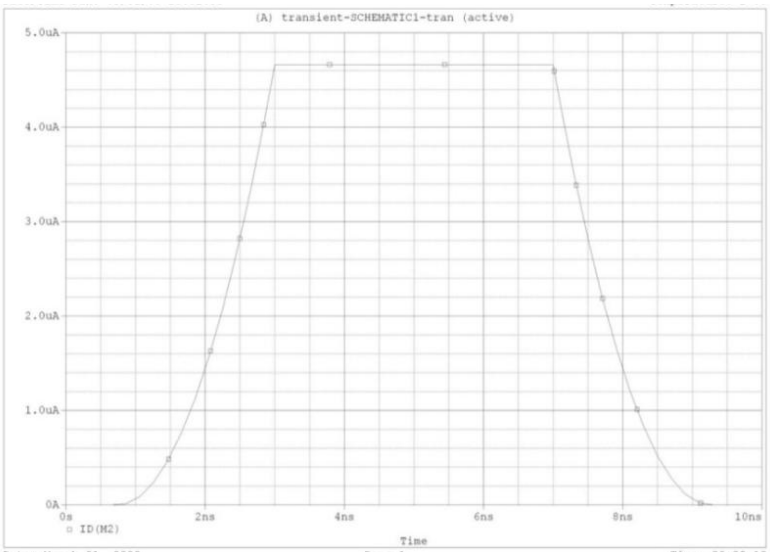


Figure: 3. A typical simulation output profile for constant voltage scaling.

Study suggests that the MOSFET drain current increases as expected with the decrease of channel length, keeping the rest of parameters constant. The drain current profiles suggest that the rise time and the fall time of the drain current is same for all channel lengths but the rate of fall is different. This contradicts the theoretical prediction that for short channel devices the rise and fall times decrease. The contradiction is because of the absence of considering all the parameter changes with the change in channel length. Next goal will be to bring about the consensus in the two results by studying different MOSFET models and figure out the incorporation of the parameters for this discrepancy.

3.2.2 Drain current with constant field scaling: Figure 4 shows a typical simulation output profile for the transient characteristics of the drain current for the channel length of 50 nm. The transient characteristics have the same shape for all different channel lengths except for the rate of fall. Here in this case threshold voltage is also scaled down along with the channel length.

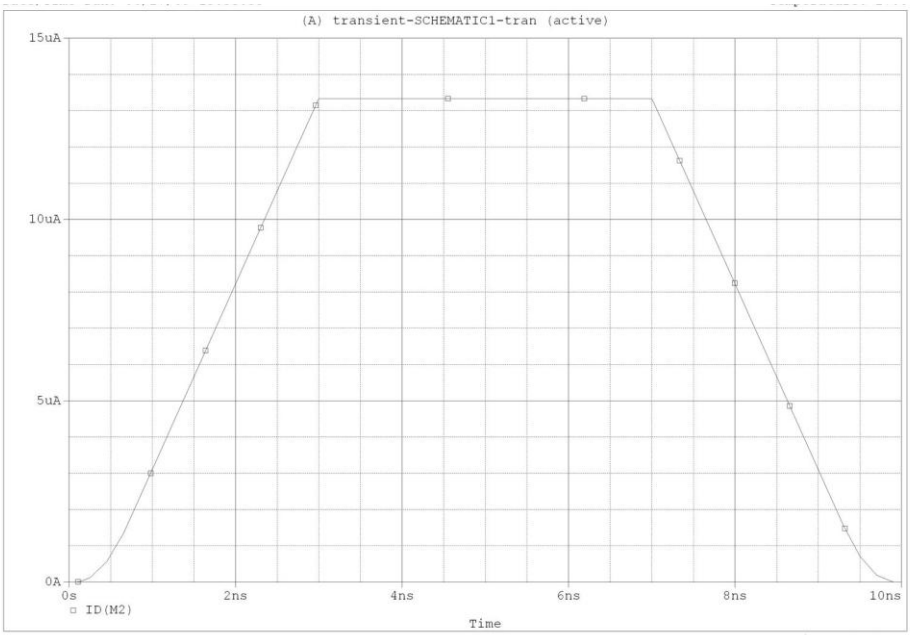


Figure 4. A typical simulation output profile for constant field scaling.

3.2.3 Drain current with general scaling: Figure 5 shows a typical simulation output profile for the transient characteristics of the drain current for the channel length of 50 nm.

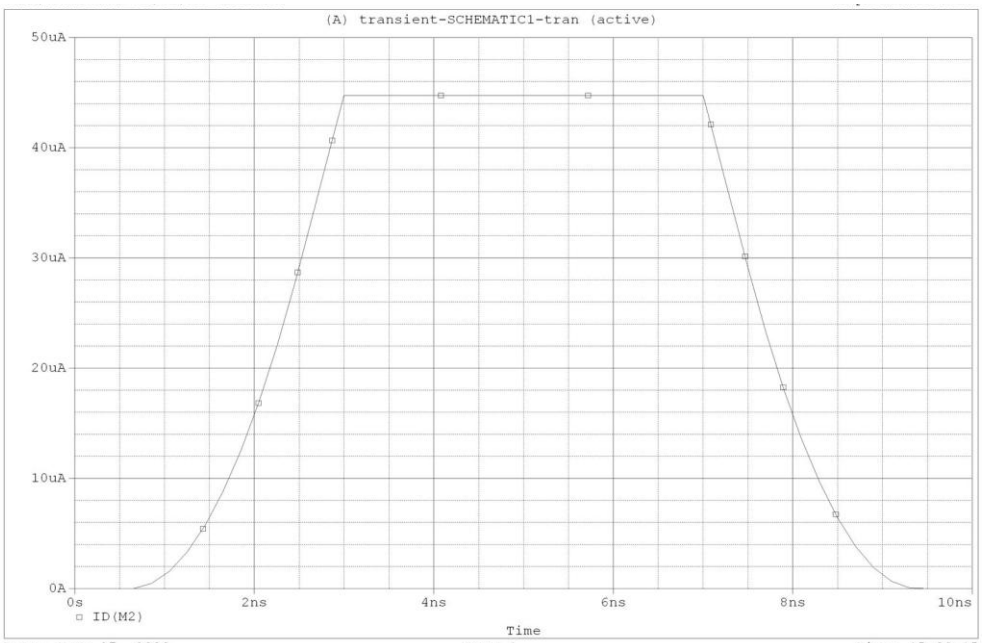


Figure: 5 A typical simulation output profile for general scaling

The transient characteristics have the same shape for all different channel lengths except for the rate of fall. In this case also the threshold voltage has been scaled down as according to the scaling trend like that of the channel length.

3.3 Graphical Analysis

To make the results, obtained for the three scaling techniques discussed above, more descriptive of the behaviour, graphs have been plotted between the peak I_D v/s channel length and the rate of its fall v/s channel length for the three scaling techniques (Figure 6 and Figure 7). These graphs help to analyze the behaviors obtained from the simulations more clearly

Figure: 6. Change in Peak I_D with the change in channel length for available scaling trends

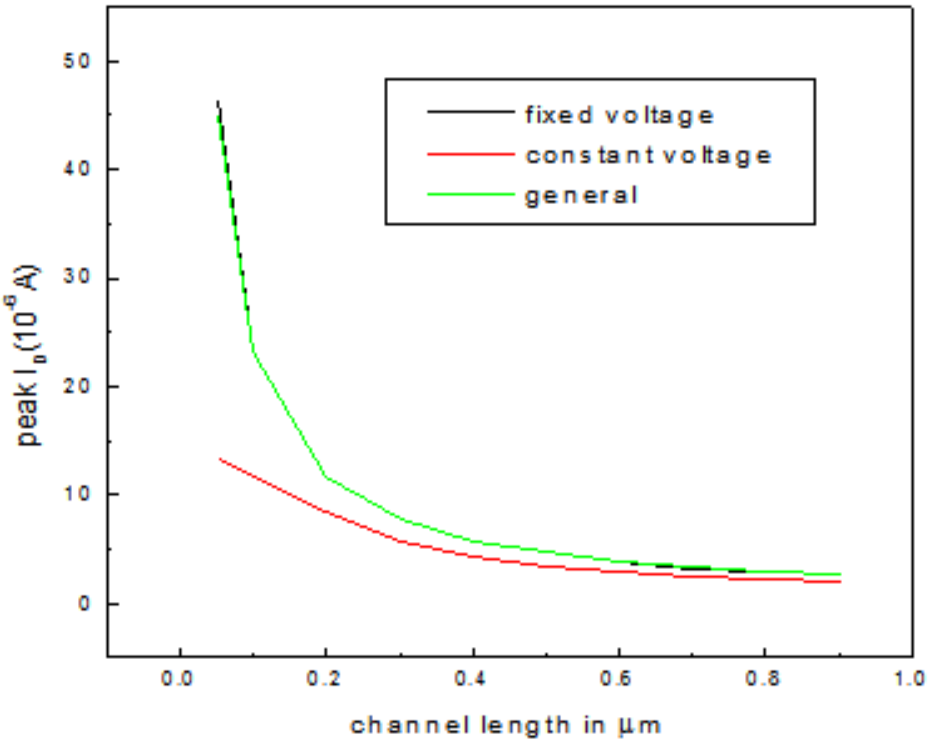
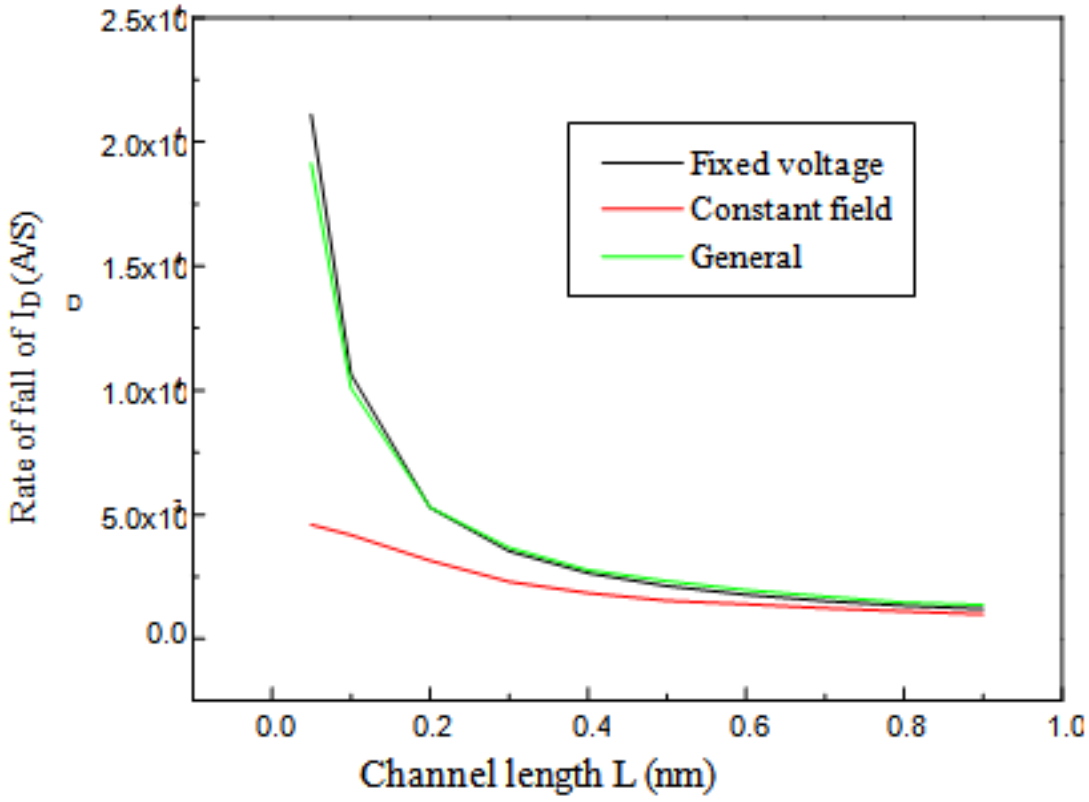


Figure 7. Rate of fall of I_D with the change in channel length for available scaling trends



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